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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,538	07/03/2003	Gary Chen	MICRON.109DC1D1	9036

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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,538	CHEN ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the c ver sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/3/03, 10/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 34, 35, and 42-44 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,957,590 to Douglas.

Regarding claims 34, 42, and 43, Douglas discloses a semiconductor stack having at least a side comprising a titanium silicide layer (22, 28; figures 2-3) having substantially etched titanium oxynitride extrusions formed on the side thereof (see column 3, lines 44-50; column 11, lines 15-20, 40-67; column 12, lines 20-30).

Regarding claims 35 and 44, Douglas discloses that the stack forms part of a transistor (figures 2 and 3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 8-14, 20-26, 32-35, and 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent Publication No. 06-021440 to Abiko in view of Douglas.

Regarding claims 1, 9, 11, 13, 21, 23, 25, 33, 34, 42, and 43, Abiko discloses a semiconductor structure comprising: a polysilicon layer (103); a barrier layer (104) comprising tungsten silicide over the polysilicon layer (paragraph 0008); a conductive layer (105) comprising titanium silicide (paragraph 0008); and a cap (107).

Abiko fails to specify that the silicide layers have substantially etched metal oxynitride extrusions.

Douglas discloses a semiconductor stack having at least a side comprising a titanium silicide layer (22, 28; figures 2-3) having substantially etched titanium oxynitride extrusions formed on the side thereof (see column 3, lines 44-50; column 11, lines 15-20, 40-67; column 12, lines 20-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the semiconductor device of Abiko has substantially etched oxynitride portions, as suggested by Douglas. The rationale is as follows: A person having ordinary skill in the art would have been motivated to substantially etch any metal oxynitride portions, because Douglas shows that metal oxynitride portions typically form as by-products of the silicidation process (Douglas, column 3, lines 30-50; column 4, line 60 – column 5, line 12), and that by etching the formed metal oxynitride portions, short circuits between the gate and source/drain regions can be prevented (column 11, lines 50-65).

Regarding claims 2, 14, 26, 35, and 44, Abiko discloses that the stack forms part of a transistor (figure 1).

Regarding claims 8, 10, 20, 22, 32, and 41, Abiko teaches that the titanium silicide must be sufficiently thick to prevent undue thinning or depletion due to oxidation (see paragraph 0005), and that the tungsten silicide layer has a higher resistivity than the titanium silicide (see paragraph 0009), but fails to specify the thickness for each silicide layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify in the device of Abiko as modified by Douglas, that the tungsten silicide layer has a thickness of about 150 angstroms, and the titanium silicide layer has a thickness of about 1000 angstroms. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide relatively thick silicide layers, in order to prevent undue thinning or complete depletion of the layer due to oxidation (see Abiko, paragraph 0005), but would also desire to provide relatively thin layers, in order to minimize the contact resistance of the gate (see Abiko, paragraph 0009), and especially minimize the thickness of the tungsten silicide layer, since its contact resistance is about five times as large as the titanium silicide (Abiko, paragraph 0009). Although Abiko doesn't specify the layer thicknesses, it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Regarding claims 12 and 24, Abiko discloses that the polysilicon layer is above a substrate comprising silicon (paragraph 0008).

5. Claims 3-5, 7, 15-17, 19, 27-29, 31, 36-38, 40, 45-47, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abiko in view of Douglas as applied to claims 1, 13, 25, 34, and 43 above, and further in view of U.S. Patent No. 6,376,348 to Schrems et al.

Abiko fails to specify the type of memory structure in which the disclosed FET is used.

Schrems teaches that FETs substantially similar to that of Abiko in view of Schrems, including a silicon substrate, a gate polysilicon layer (121) and metal silicide layer (122) are used in SDRAMs, static memory devices, dynamic memory devices, and wordlines for memory devices (column 3, lines 13-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the FET of Abiko as modified by Douglas is used as part of a SDRAM, SRAM, DRAM, or wordline structure, as suggested by Schrems. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use the FET of Abiko in view of Douglas with the specified memory structures, because the FET of Abiko as modified by Douglas provides low contact resistance (see Abiko, paragraphs 0005-0009) and relative immunity to undue gate to source/drain shorting (Douglas, column 11, lines 50-65). Since the specified memory structures have substantially the same FET structure (see Schrems, figure 1), it is well within the purview of a person having ordinary skill in the art to use the FET of Abiko as modified by Douglas in any of the structures in order to achieve the benefits mentioned supra.

6. Claims 6, 18, 30, 39, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abiko in view of Douglas as applied to claims 1, 13, 25, 34, and 43 above, and further in view of Schrems et al. and U.S. Patent No. 6,097,660 to Tsuchida et al.

Abiko is silent as to the nature of the memory structure in which the disclosed FET is used.

Schrems teaches that FETs substantially similar to that of Abiko in view of Schrems, including a silicon substrate, a gate polysilicon layer (121) and metal silicide layer (122) are used in DRAMs (column 3, lines 13-23).

Tsuchida et al. further teaches that extended data out memories refer to a common mode of operation for DRAM devices for high speed operations (column 1, lines 25-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the FET of Abiko as modified by Douglas is used in a DRAM, as suggested by Schrems, operating in an extended data out mode, as suggested by Tsuchida. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use the FET of Abiko in view of Douglas in an EDO DRAM device, because Schrems teaches that a FET having substantially the same structure as that of Abiko is used in a DRAM (Schrems, column 3, lines 13-23; figure 1), and Tsuchida teaches that an EDO DRAM should have the advantage of higher speed operation, but should also have substantially the same FET configuration as any other DRAM, and hence, substantially the same configuration as that disclosed by Abiko (see Abiko, column 1, lines 25-40). Since the FET of Abiko in view of Douglas provides low contact resistance (see Abiko, paragraphs 0005-0009) and relative immunity to undue gate to source/drain shorting (Douglas, column 11, lines 50-65), it is well within the purview of a person skilled in the art to use this FET in an EDO DRAM, in order to achieve the FET advantages, as well as provide high speed memory operation.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,723,893 to Yu et al. discloses a gate structure using two silicide layers.

b. U.S. Patent No. 4,897,287 to Berger teaches the removal of TiON formed after silicidation.

c. U.S. Patent No. 6,013,569 to Lur et al. teaches a transistor structure in which the unreacted metal is removed from the substrate after a silicidation process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Carl Whitehead

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd